ERCIM "Alain Bensoussan" Fellowship Scientific Report

Fellow: Atanas Nikolov Kostadinov
Visited Location : NTNU, Norway
Duration of Visit: 9 months (10th of January, 2007 – 9th of October, 2007)

I - Scientific activity

I have worked with my Supervisor (Professor DSc. Guennadi Kouzaev) in the predicate logic (PL) field during the whole time of ERCIM Fellowship Programme.

We have started our collaboration even before my arrival in NTNU using e-mails. At this period, we talked about our future cooperative work. We have outlined the basic tasks, which are possible to solve during fellowship period. I have proposed and applied successfully for DE2 (Development and Education 2) board donation. In this way, it has been ensured contemporary FPGA (Filed Programmable Gate Array) board used later as a main development tool in our scientific work.

When I arrived in NTNU, it was necessary to get more knowledge about mathematical background connected to PL. I have read some additional books, scientific materials and a paper done by Professor Kouzaev connected to his pioneering work in truth-tables of PL gates. Then we have started synthesizing the predicate AND, OR and NOT logic gates using CPLD (Complex Programmable Logic Device) board UP2 (University Program 2) and Quartus® II software produced by ALTERA Corp. The work has been finished after their successful verification using an oscilloscope and input stimuli produced by switches located on the same CPLD board. We have written the first paper for the ERCIM Fellowship period with collected results obtained in the development and testing processes. The paper has been presented on a conference. After finishing this work, we have proposed a scientific project to the Norwegian Research Council. The name of the project is Development of a Real-time Reconfigurable Microprocessor for High-speed Seamless Wireless Telecommunications. This project would be a naturally extension of the work carried out during our cooperation.

Then we have continued with realizing of PL combinational and sequential components and predicate logic processor (PLP). The design process has been based on the donated DE2 board and new versions of Quartus® II specialized software especially SignalTap II Embedded Logic Analyzer all of them produced by ALTERA Corp. After their successful verification, with collected results of our work has been created an article for an American science journal. In this article has been given summarized information about the whole research work done during ERCIM Fellowship period concerning the predicate gates, predicate hardware components and PLP, the way of their design and verification, etc. The proposed article has been submitted for a review.

There is another possibility for publishing of our results. We are looking for invitation to send extended version of our first conference paper. In case of positive reviews the proposed article will be included in a book published by Springer Verlag.

At the end, after finishing the ERCIM Fellowship we will keep in touch with my Supervisor Professor Kouzaev. My expectations are that our useful cooperation will continue. We are able to realize new science papers and articles based on the experience in predicate logic field as well as in another interesting and promising scientific topics.

II- Publication(s) during your fellowship

Please insert the title(s), author(s) and abstract(s) of the published paper(s). You may also mention the paper(s) which were prepared during your fellowship period and are under reviewing.

The title of the published paper is Predicate Gates for Spatial Logic (paper number: 561-162).

The authors of the paper are Guennadi A. Kouzaev and Atanas N. Kostadinov.

The content of the abstract is given on the next lines.

The predicate logic gates are proposed for spatially modulated signals. Two voltage impulses are transmitted along the coupled wires, and they are considered as a predicate expression. The developed gates perform the logical operations AND, NOT and OR with these expressions. They are used for a predicate logic microprocessor.

The above-mentioned paper has been presented on the 11th WSEAS International Conference on COMPUTERS, July 26-28, 2007 in Agios Nikolaos, Crete Island, Greece.

The title of the submitted article is Predicate Gates, Components and a Processor for Spatial Logic.

The authors of this article are Guennadi A. Kouzaev and Atanas N. Kostadinov. It has been submitted for a review and publication in American Journal JCSC (Journal of Circuits, Systems, and Computers).

The content of the abstract is given on the next lines.

The predicate logic gates, components and a processor are proposed for spatially modulated signals. Two voltage impulses are transmitted along the coupled wires and considered as a predicate expression. The developed gates and processor perform the predicate logical operations AND, NOT and OR with these expressions. For the design of predicate gates, components and processor are used CPLD and FPGA boards and corresponding software. The all proposed electronic circuits are verified successfully. The designed processor is compatible with the classical computers and applicable to the artificial intelligence area as linguistic calculations, database machines and SQL servers, etc.

As I mentioned in scientific activity chapter we are waiting for invitation to be send an extended version of our first conference paper. In case of positive reviews, the proposed article will be included in a book published by Springer Verlag.

III -Attended Seminars, Workshops, and Conferences

Please identify the name(s), date(s) and place(s) of the events in which you participated during your fellowship period.

I participated in Assessment Week workshop. It has taken place in NTNU, between 4 – 8 June. There have been presented materials connected to the way of doing of the assessment process in James Madison University (JMU), USA.

I participated also in the 11th WSEAS International Conference on COMPUTERS. Is has been held at 26 till 28 of July 2007 in Agios Nikolaos, Crete Island, Greece. There, I introduced the paper entitled Predicate Gates for Spatial Logic (paper number: 561-162).