ERCIM "ALAIN BENSOUSSAN"
FELLOWSHIP PROGRAMME

Scientific Report

First name / Family name	Azamolsadat Seyedi
Nationality	Iranian
Name of the *Host Organisation*	Norwegian University of Science and Technology (NTNU)
First Name / family name of the *Scientific Coordinator*	Per Gunnar Kjeldsberg
Period of the fellowship	01/05/2017 to 30/04/2018

I – SCIENTIFIC ACTIVITY DURING YOUR FELLOWSHIP

I prepared a proposal and submitted it to get Marie-Curie Individual Fellowship with the support of my host, Prof. Per Gunnar Kjeldsberg, and the Faculty of Information Technology and Electrical Engineering at NTNU. The proposal has been accepted to get funding; accordingly, it will be active for the next three years (2018-2021). The proposal name is PALMERA, which addresses the low power and fault tolerant cache memory design bottlenecks through a combination of hardware and software approaches.

I spent most of summer days to complete the proposal until 14th of September 2017, the deadline day. During proposal preparation, I performed a substantial literature review to get enough information about state of the art memory designs and technologies, especially level-one cache memories that are activated at each memory access, and therefore critical components for designing future microprocessors. The design of low power and fault tolerant caches has a rich body of work at different design abstraction levels. I concentrated on papers that had investigated circuit and system level techniques to improve the reliability during voltage scaling when drastic increase in the number of memory cell failures happen. Indeed, the proposal research direction is to develop a cache memory hardware, which is equipped with novel circuit designs to keep the reliability during voltage scaling. This design allows us

to operate down to near-threshold voltage levels while trading off cache capacity for power saving.

Exploring radiation effects on memory cell resilience was my other concern during the study phase. The environment is full of charged particles and cosmic rays that can cause unexpected effects on electronic circuits. At the same time, the scaling in recent memory technologies makes the circuits more sensitive to radiation effects, as the needed charge to cause a bit to flip is reduced. Therefore, I studied recent papers investigating radiation tolerance of emerging memory technologies to improve the reliability of computing systems. While preparing the proposal, I mostly focused on memories implemented for embedded systems of areas such as space applications where the level of radiation is very high; hence, adding advanced techniques to deal with the reliability issues during voltage scaling is critical here.

The types of applications in focus by PALMERA, space application systems, are increasingly becoming multitasked and dynamic; hence, data intensive and fluctuating with respect to resource requirements due to their inherent dynamism. Therefore, available static analysis and worst-case design margins cannot meet the power and reliability constraints present in such embedded systems. Hence, during the study phase, I surveyed articles proposing the so-called System Scenario based Design Methodology that has been developed to optimize energy consumption of dynamic systems at run time. System scenario-based techniques enable exploitation of application dynamism through fine-grained run-time system tuning. In fact, the main goal of PALMERA is to leverage a combination of circuit level and run time level techniques to simultaneously handle unreliability and reduce power consumption.

After submitting the proposal, I started to update my knowledge in circuit design, especially analog circuit and system design since I had concentrated on FPGA design for several months. I read Analog and Digital circuit books and I listened to online available courses. Meanwhile, I surveyed several tutorials. Later on, I started first part of the project, looking for new techniques, whether at circuit or architecture level, that could mitigate fault rate increase during voltage scaling. Finally, I decided to design a memory with FD-SOI technology and apply different body biasing voltage levels to control power consumption and leakage current. Body biasing is the key feature of FD-SOI technology enabling a combination of high performance and low power for optimum energy efficiency. It consists of applying a voltage in order to shift each transistor threshold voltage to either gain in performance or reduce the leakage power consumption. Afterwards, I have started to design an 8-KB memory with 28-nm FD-SOI technology at 2GHz processor frequency and 1V supply voltage. During voltage scaling, the fault rate is calculated and the proper body biasing voltage is applied to mitigate the noise effects in SRAM cells. Furthermore, the cell's resilience is reinforced by applying data duplication/triplication techniques in middle and low voltage levels. In February, we received notice that Marie-Curie proposal got funding and I could continue working on this project for the next three years.

Since the project had two research directions, circuit level and system level, I registered to Computer Architecture course that was held in the spring semester (January to April 2018). Through this course, I could increase my knowledge in the computer architecture fundamentals. Furthermore, a mandatory course project had to be done with M5 simulator that could help me to increase my knowledge in practical system design.

II – PUBLICATION(S) DURING YOUR FELLOWSHIP

Under Preparation:

Azam Seyedi, Even Late, Snorre Aunet, Per Gunnar Kjeldsberg, 'Exploiting Dynamic Body-Biasing Effects on Reliability of Low-Power 8KB FD-SOI Cache Memory Design during Voltage Scaling'

Azam Seyedi, Per Gunnar Kjeldsberg, 'Low-Power and Fault-Tolerant Cache Memory Design through a Combination of Hardware and Software Approaches'

III – ATTENDED SEMINARS, WORKHOPS, CONFERENCES

1- FPGA-forum 2018, 14-15. February 2018, Royal Garden, Trondheim.
2- Deep Learning with MATLAB, Mathwork Workshop in conjunction with FPGA Forum, 13 February 2018
3- Energy Efficiency Seminar hosed by The Energy Efficient Computing Systems group at NTNU, June 7, 2017.
4- ICT workshop - kick-off Horizon 2020 work programmes 2018-2020, 16 October 2017.
5- H2020 Proposal Development Course, 11 October 2017

IV – RESEARCH EXCHANGE PROGRAMME (REP)

From the 13th to the 20th of March 2018, I visited the Computer Architecture and VLSI Systems (CARV) Laboratory at FORTH ICS in Greece. CARV promotes research in the design and implementation of computing systems such as scalable architectures, parallel programming & software, and storage & I/O subsystems. My host was Professor Manolis Katevenis at University of Crete. During my visit, I got opportunity to meet him as well as his PhD and postdoc researchers. We engaged in exchange of ideas on the run-time level optimization in embedded systems. Ideas for possible joint research activities were put forward during the visit.