




# Scientific Report

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| Nationality | Polish |
| Name of the *Host Organisation* | NTNU |
| First Name / family name of the *Scientific Coordinator* | Leif Arne Rønningen |
| Period of the fellowship | 01/10/2011 to 30/09/2012 |

# I – SCIENTIFIC ACTIVITY DURING YOUR FELLOWSHIP

During my fellowship I have conducted research on FPGA-based platform for the for DMP (Distributed Media Plays) network node during supervision of Prof. Leif Arne Rønningen.
DMP is the futuristic telepresence system which is aimed at providing near-natural virtual meeting environment between users hosted in collaboration spaces. There are a number of applications for which DMP may prove useful. These include, but are not limited to, musical sessions, song lessons, distributed opera, multi-player games, near natural virtual meetings and remote surgery. The collaboration spaces proposed by DMP give the perception that the communicating parties are in the same physical space, as nearly as possible, by having 3D auto-stereoscopic multiview video and multi-channel sound.
The network node is implemented hardware to give the minimum possible end-to-end delay for routing and performing other network-related functionalities. In order to enable flexible extension of the system FPGA-based platform adopts AXI-bus standard.
The set of hardware modules were designed such as the dropping module which is a part of quality shaping scheme.

The core accomplishments during my fellowship:

- Design and implementation of the FPGA-based platform for DMP
- Design and analysis of the FPGA-based architecture for the Kriging interpolation module
- Implementation of a low-latency driver for PCIe communication between FPGA and server platform
- Design and implementation of user space application for server communication in DMP
- Design and implementation of the dropping module for DMP

# II – PUBLICATION(S) DURING YOUR FELLOWSHIP

- **FPGA-based platform for real-time Internet**
  Maciej Wielgosz, Mauritz Panggabean, Ameen Chilwan, and Leif Arne Rønningen
  3rd International Conference on Emerging Security Technologies (EST) 2011
  Lisbon, Portugal, 5-7 Sep 2012 – published

**Abstract**
Field-programmable gate arrays (FPGAs) are widely used in telecommunication due their substantial computational power and flexibly designed architecture. These features become especially important for applications of low transmission latency such as those supported by Distributed Multimedia Plays (DMP) architecture. Thus FPGAs are chosen in this work as the core building block of the system. Complex multi-node telecommunication systems require special design methodology contrary to small ICT applications usually implemented in HDL. The methodology should be based on the appropriate tools from FPGA vendors for support and maintenance. This paper presents an architecture of a module to be embedded in all the FPGA-based nodes constituting a platform for the Real Time Internet based on

DMP. It is designed using an embedded development kit natively supported by Xilinx and flexible in available cores. We present the implementation results of the network-node module and the description of PCIe-based protocol for inter-FPGA communication.

- **An FPGA-based platform for a network architecture with delay guarantee**
  Maciej Wielgosz, *Mauritz Panggabean*, Jiang Wang and Leif Arne Rønningen
  *Submitted to Journal of Circuits, Systems and Computers – pending*

**Abstract**
The background that underlies this work is the envisioned real-time tele-immersive collaboration system for the future that supports delay-sensitive applications involving participants from remote places via their collaboration spaces (CSs). The end-to-end delay as high as 20 ms is required for good synchronization of such applications, for example collaborative dancing and remote conducting of choir. It is much lower than that facilitated by existing teleconference systems. A novel network architecture with delay guarantee, namely Distributed Multimedia Plays (DMP), has been proposed and designed to realize the vision. The maximum low latency is guaranteed because DMP network nodes can drop DMP packets of multimedia data from the CSs due to instantaneous tra_c condition. Besides ultrafast processing time, modularity and scalability must be taken into account in hardware design and implementation of the nodes for seamless incorporation of the modules. These lead us to employing field-programmable gate array (FPGA) due to its substantial computational power and exibility. This paper presents an FPGA-based platform for the design and implementation of DMP network nodes. It provides a detailed introduction to the platform architecture and the simulation-implementation environment for the design. The modularity of the implemented node is shown by addressing three important modules for packet dropping, 3D warping, and image transform. Our compact implementation of the network node on Xilinx Virtex-6 ML605 mostly consumes very small amount of available resources. Moreover the elementary operations on our implementation takes (much) less than 5 _s as desired to meet the low-latency requirement.

- **FPGA Architecture for Kriging Image Interpolation**
  Maciej Wielgosz, *Mauritz Panggabean* and Leif Arne Rønningen
  *Submitted to International Journal of Signal and Imaging Systems Engineering - pending*

**Abstract**
This paper presents an analysis of Kriging algorithm with respect to FPGA implementation and the architecture proposal for a hardware module. The module is to be used in Distrbued Multimedia Plays (DMP) as a part of quality shaping scheme (QS). The algorithm as a whole is not well suited for FPGA but the authors came up with a concept for the algorithm division to address this challenge. The idea leverages the profile of data the algorithm operates on to reuse some of the calculations and skips highly exhaustive computations. It was shown that despite a high complexity of the algorithm it is possible to process images of 256x256 pixels in a reasonable time (< 1ms). Described module is a part of a bigger system therefore keeping low FPGA resources usage was imperative and this objective was achieved. The design was focused on low latency of the module rather than processing throughput which may justify some of the

adopted strategies. The proposed architecture is both flexible and modular which enables migration across different platforms.

- **Incorporating DCT-based image compression into a delay-guaranteeing network architecture**
  *Mauritz Panggabean*, Maciej Wielgosz, Leif Arne Rønningen and Harald Øverby
  *To submit to IEEE Transactions on Circuits and Systems for Video Technology*

## III – ATTENDED SEMINARS, WORKHOPS, CONFERENCES

- 3rd International Conference on Emerging Security Technologies (EST) 2011 Lisbon, Portugal, 5-7 Sep 2012
- Biweekly team seminars

## IV – RESEARCH EXCHANGE PROGRAMME (REP)

1. Exchange visit 22-26.08.2012
   Center director, Bengt Ahlgren, Communication Networks & Systems laboratory at SICS Center for Networked Systems. Sweden.

   During my visit I gave a talk on FPGA-based platform on DMP focused mostly on latency control and monitoring in high-throughput networking systems. My presentation addressed the most vital aspects of designing low-latency systems in FPGAs. The team of Bengt Ahlgren deals with different strategies on data caching in networked systems which requires profound analysis and consideration of buffers and introduced latency.
   The visit was very beneficial and created a prospect for a future research.
2. Exchange visit 04-10.09.2012
   Prof. Nuno Rom, IST/INESC-ID, Technical University of Lisbon, Dept. of Electrical and Computer Engineering.

   During my visit to INESC-ID I gave a talk about FPGA-based platform for Real-Time Internet. There were several aspect of the project which attracted a special attention. One of them was compression by network as a video processing system. I have learned about the research conducted at INESC-ID related to a design of a new architectures on parallel DNA sequencing.